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(54) **Semiconductor integrated circuit for neural network**

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Description

Background of the Invention:

The present invention relates to semiconductor integrated circuits, and more particularly to a semiconductor integrated circuit which is well suited to form a neural network model in the shape of a monolithic IC.

A neuron consists of a soma, a dendrite and an axon. Of them, the soma generates a pulsing voltage output when its internal potential has risen to exceed a certain threshold value. The pulse voltage is transmitted through the axon until it reaches the distal end of a nerve. The nerve end lies in contact with the dendrite or soma of another neuron. The point of the contact is called a "synapse". The transmission of information between the neurons is effected through the synapse. Such synapses are classified into two sorts; a synapse which has the property of raising the internal potential of the soma of the opposite neuron (hereinbelow, expressed as an "excitatory synapse"), and a synapse which has the property of lowering the internal potential of the soma of the opposite neuron (hereinbelow, expressed as an "inhibitory synapse"). A plurality of synapses are connected to one neuron, and when the pulse reaches one excitatory synapse, the internal potential is caused to rise and then gradually fall in accordance with a certain time constant by the synapse. When the pulses reach one synapse continuously, their potentials are successively added with the lapse of time. On that occasion, the arriving pulses have plus or minus weights assigned thereto, depending upon whether they are the excitatory or inhibitory synapses. Therefore, the value of the internal potential becomes the weighted sum of all the inputs. When this value exceeds the threshold value, the neuron generates the pulsing output.

Information processing within the brains of human beings etc. is conducted by a network which is constructed with such a neuron as a unit. Heretofore, in order to explicate the algorithm of the information processing within the brains, researches have been made by modeling the neural network in hardware or software implementation and by performing various aspects of information processing.

Meanwhile, with the progress of semiconductor integrated circuits, researches for realizing the neural network models on semiconductor chips have recently been made vigorously. They are detailed in, for example, "Researches on and Developments of Neurocomputers", NIKKEI ELECTRONICS (dated January 26, 1987, pp. 159 - 170). The "neurocomputer" mentioned above signifies a computer which is suitable for parallel processing imitative of the operations of the brain of the human being. That is, it achieves the high-speed processing of pattern recognition, combinatorial problems, etc. while utilizing the parallel processing function which is one of the features of the neural network.

Figs. 7(a) and 7(b) are a symbolic diagram of a neuron, and a graph showing the input/output relationship of the neuron, respectively.

In general, a neural network model is constructed of an element of many inputs and one output (hereinbelow, called "neuron") as shown in Fig. 7(a). The respective input terminals of the neuron are given the values of outputs from another neuron. On that occasion, the inputs are multiplied by predetermined weights owing to the functions of the connection parts (hereinbelow, written as "synapses") between the neurons, whereupon the resulting products are afforded to a soma (hereinbelow, written as "cell") 1. Fig. 7(a) shows the symbols of this neuron, and the two sorts of synapses; excitatory synapses 21 having plus weights and inhibitory synapses 22 having minus weights are illustrated.

As stated before, the input/output relationship of the neuron is expressed by the weighted sum of voltages which rise in accordance with a certain time constant. More specifically, as illustrated in Fig. 7(b), the output OUT becomes a function of the summation ($\Sigma_i W_i \cdot P_i$) of the products between all the inputs (P_1, P_2, ..., P_i, ... and P_n) and the weights (W_1, W_2, ..., W_i ... and W_n) of the synapses lying at the respectively corresponding input ends.

When a plurality of neurons are coupled to one another and the weights of the individual synapses are appropriately selected, the resultant network can perform significant information processing.

An example of the neural network model as expressed using an electrical circuit is Hopfield's model. In this model, resistors are used for expressing the weights, and gate circuits are used for expressing an input/output relationship similar that of Fig. 7(b).

Fig. 8 is a diagram showing the Hopfield model in the prior art.

This diagram is a model diagram illustrated in U. S. Patent No. 4660166. In the figure, the mark of a black square indicates a resistor which expresses the synaptic weight between two lines intersecting at the corresponding point, and the marks of a gate and an inverter gate indicate excitatory and inhibitory set inputs and outputs, respectively. The input weights and the connection goals of the plus and minus outputs for three neurons are illustrated in Fig. 8.

In general, in a neural network model, it is sometimes the case that, when synaptic weights are changed on and on in accordance with a predetermined algorithm, they are respectively converged to certain values.

Such an operation is usually called "learning".

Several methods have been proposed for the algorithm of the learning. In any case, however, the synaptic weights need to be altered.

US-A-3 476 954 discloses a circuit for constructing a neural network model with the features included in the first part of claim 1.

In the prior art mentioned above, the synaptic weights are expressed by resistors, and corrections of the synaptic weights require alteration of the resistances. Therefore, if the circuit is an integrated circuit, all processes must be redone from the layout of the IC, so that alteration of learned contents becomes difficult.

It is an object of the present invention to provide a circuit for constructing a neural network model in which synoptic weights can be readily altered at need, and which can realise a neuron circuit by a monolithic IC.

The invention meets this object by the circuit defined in claim 1.

According to this construction, one synapse is expressed by one current switch and one current source circuit, the value of the current which is caused to flow into the current switch by each current source circuit corresponds to one synaptic weight, and this current value can be externally controlled. Therefore, the synaptic weights can be easily altered by the voltages or the likes applied from outside.

In addition, the value of the total current of all the regulated current soruces which afford the synaptic weights is held constant by the other requlated current source separately provided, so that when the current values of some regulated current sources are to be increased by the external voltages, the currents of the remaining regulated current sources decrease inevitably. Since the currents of the respective regulated current sources express the synaptic weights, it is imposed as a restriction in the present invention that the summation of the synaptic weights is constant.

The latter feature is of interest because when a learn ing operation of a neural network model is subjected to the restriction that the summation, or the sum of the squares, of the weight of synapses connected to one neuron is constant, the learning result is sometimes enhanced. While this was known from researches employing computer simulations, the effect was not considered by the prior-art circuit referred to above.

Brief Description of the Drawings:

Fig. 1(a) is a diagram showing the outline of a semiconductor integrated circuit in an embodiment of the present invention, Fig. 1(b) is a symbolic diagram corresponding to Fig. 1(a), Fig. 1(c) is a diagram showing the details of a synaptic circuit in Fig. 1(a), Fig. 1(d) is a graph showing an example of the saturation function $f(P_i)$ of the synaptic circuit with respect to the input signal P_i thereof, and Fig. 1(e) is a diagram showing a circuit for realizing the characteristic in Fig. 1(d);

Fig. 2 is a diagram showing the arrangement of a regulated current source portion in the synaptic circuit of the present invention;

Fig. 3 is a diagram showing another arrangement of the synaptic circuit of the present invention;

Fig. 4 is a diagram showing the regulated current source portion of the synaptic circuit in Fig. 3;

Fig. 5 is a diagram showing another semiconductor integrated circuit according to the present invention;

Fig. 6(a) is a model diagram of a synaptic circuit shown in Fig. 5, Fig. 6(b) is a symbolic diagram of a neural network which employs the semiconductor integrated circuit in Fig. 5, and

Fig. 6(c) is a symbolic connection diagram of the neural network in Fig. 6(b);

Fig. 7(a) is a symbolic diagram of a neuron, while Fig. 7(b) is a graph showing the input/output relationship of the neuron; and

Fig. 8 is a diagram showing Hopfield's model in the prior art.

Description of the Preferred Embodiments:

Now, embodiments of the present invention will be described in detail with reference to the drawings.

Fig. 1(a) is a block diagram of a semiconductor integrated circuit (neuron) showing an embodiment of the present invention.

In Fig. 1(a), symbols 2-1 and 2-2 denote synaptic circuits each of which includes n synapses. The circuit 2-1 connected to the + side (noninverting input terminal) of a differential amplifier 11 is an excitatory synapse circuit, while the circuit 2-2 connected to the - side (inverting input terminal) is an inhibitory synapse circuit. Besides, Fig. 1(b) is a diagram in which Fig. 1(a) is symbolically expressed. Parts P_1 - P_n and P_1' - P_n' provided in the individual synaptic circuits 2 are input terminals to which external inputs or the outputs of another neuron are respectively connected. Here, the input terminals P_1 - P_n signify ones which are associated with excitatory synapses having weights W_1 - W_n, while the input terminals P_1' - P_n' signify ones which are associated with inhibitory synapses having weights W_1' - W_n'.

Fig. 1(c) is a diagram showing the details of the synaptic circuit 2-1 or 2-2. Referring to the figure, each input is connected to the base of the transistor Q_{i2} of a current switch which is configured of a pair of transistors Q_{i1} and Q_{i2} (i = 1 - n). The other inputs (the bases of the transistors Q_{i1}) of such current switches are all supplied with a fixed voltage V_{BB}. In addition, the emitters of each pair of transistors Q_{i1} and Q_{i2} are both connected to the collector of a transistor Q_{si} underlying the paired transistors. The transistor Q_{si} and a resistor r underlying this transistor operate as a regulated current source. That is, a current I_i of certain fixed value corresponding to the base potential W_i of the transistor Q_{si} flows through this transistor Q_{si}.

When the i-th input P_i has become sufficiently greater than the voltage V_{BB}, the current I_i corresponding to the potential W_i flows from a resistor R to a voltage terminal V_{EE} via the transistor Q_{i2}. To the contrary, when the input P_i has become sufficiently smaller than the voltage V_{BB}, the current I_i flows from a GND (ground) point to the terminal V_{EE} via the transistor Q_{i1}. Besides, in a case where the input P_i is near the voltage V_{BB}, the current whose value is proportional to the magnitude of the input P_i flows through the resistor R.

The resistor R is connected to all the current switches, so that when currents based on the plurality of inputs P_i flow at the same time, the summation current thereof flows through the resistor R. That is, letting Vo denote the output of the synaptic circuit 2, the following holds:

$$V_o = -R\left(\sum_{i=1}^{N} I_i \cdot P_i{*}\right) \qquad \cdots (1)$$

In the above formula, $P_i{*}$ denotes a variable which becomes "1" when the input voltage to the terminal P_i is sufficiently greater than the voltage V_{BB}, which becomes "0" when the former is sufficiently smaller than the latter, and which becomes a value between "1" and "0" in proportion to the input voltage when the former is near the latter. A function $f(P_i)$ which gives the variable $P_i{*}$ is as shown in Fig. 1(d) and has a shape similar to that of the function in Fig. 7(b), and the details thereof are determined by the characteristics of each pair of transistors. By way of example, as illustrated in Fig. 1(e), resistors r_d are inserted into the emitter coupling parts of each pair of transistors Q_{i1} and Q_{i2} (i = 1 - n) constituting the current switch, and the resistances thereof are changed. Then, a rectilinear region corresponding to input voltage values near the voltage V_{BB} can be widened or narrowed in the characteristic depicted in Fig. 1(d). When the resistors r_d employed are ones, such as pinch resistors, the resistances of which can be changed by a voltage V_d, the saturation function $f(P_i)$ (in Fig. 1(d)) which is exerted on the input can be dynamically varied during the operation of the circuit.

Besides, I_i in Eq. (1) denotes the value of the current which is controlled by the i-th current switch. This value corresponds to the base potential W_i of the transistor Q_{si} included in the i-th regulated current source. Assuming here that the potentials W_i correspond to the synaptic weights, the output V_o in Eq. (1) may be regarded as indicating the summation of the products between the synaptic weights and the inputs.

Eventually, the summations of the products between the synaptic weights and the inputs are respectively provided by the excitatory and inhibitory synapse circuits and are respectively applied as the noninverting and inverting inputs of the differential amplifier 11 so that the output of this differential amplifier 11 may be proportional to the difference of the two inputs. Thus, the summation of the products between the weights and the inputs at all the synaptic nodes is obtained. Subsequently, this output is applied to the synaptic circuit of another neuron and is subjected to the function as shown in Fig. 1(d). Therefore, the circuit in Fig. 1(a) operates as one neuron.

When the neuron is expressed by such a construction, the synaptic weights W_i are expressed by the potentials which are externally applied to the bases of the transistors Q_{si} within the synaptic circuits 2, and the values of the weights can be altered with ease.

The second embodiment of the present invention is such that the regulated current source array 3 in the synaptic circuit 2 of the first embodiment described above is replaced with an arrangement employing MNOS transistors (metal-nitride-oxide-semiconductor transistors, namely, MOS transistors each having a floating gate) as shown in Fig. 2.

A pulse voltage is impressed on the gate of the MNOS transistor for a period of time corresponding to the synaptic weight W_i (i = 1 - n). A drain current I_D which flows through the MNOS transistor increases substantially in proportion to the duration of the pulse voltage which is impressed on the gate. Moreover, once the current I_D has been set by the impression of the pulse, the value thereof remains constant until a pulse is subsequently impressed again.

Accordingly, whereas any contrivances for keeping the values of the weights W_i constant are necessitated outside the array 3 in the number of the synapses in the first embodiment, they are dispensed with in the second embodiment, to bring forth the effect that the arrangement of the whole circuit can be simplified.

Fig. 3 shows the third embodiment of the present invention. The point of difference from the first embodiment is that a total current which the regulated current source array of the synaptic circuit causes to flow is held constant by a regulated current source circuit I which is separately provided. Thus, in the synaptic circuit of the third embodiment, the currents I_i of values corresponding to the weights W_i (i = 1 - n) flow through the respective current switches, but the summation thereof is always held constant. In other words, the summation of the weights W_i is held constant without fail.

The fourth embodiment of the present invention consists in that the portion of the regulated current source transistor array 3 in the synaptic circuit 2 shown in Fig. 3 is replaced with an array of transistors as shown in Fig. 4, the base potentials of which are made common and the emitter areas of which are respectively changed in accordance with the values of currents intended to flow. In this embodiment, the values of the regulated currents corresponding to the synaptic weights are respectively determined by the emitter areas of the individual regulated current source transistors. Accordingly, it is impossible to externally and freely change the regulated current values corresponding to the synaptic weights as in the first to third embodiments, and the weights are determined by a pattern in the process of manufacture. However, this embodiment has many merits in the points of the scale and cost of the device, and both the types are properly used depending upon applications.

Incidentally, in the third and fourth embodiments respectively shown in Figs. 3 and 4, the resistors $\underline{r}$ as depicted in Fig. 1(c) are not connected to the emitters of the transistors constituting the regulated current source arrays. It is to be understood, however, that quite similar operations proceed even when the resistors $\underline{r}$ are connected.

Fig. 5 is an arrangement diagram of a semiconductor integrated circuit (neuron) showing the fifth embodiment of the present invention.

Referring to Fig. 5, numeral 2 (symbol 2-1 or 2-2) indicates one synapse, to which one or more other synapses are connected through a common addition line of + side or - side. The + side addition line executes the addition of the excitatory synapse, while the - side addition line executes the addition of the inhibitory synapse. Parts A_1 - A_8 or B_1 - B_8 provided in the single synapse 2-1 or 2-2 are input terminals to which other neuron outputs are respectively conencted. Here, the input terminals A_1 - A_8 are ones of the excitatory synapse, while the terminals B_1 - B_8 are ones of the inhibitory synapse. The synapse 2 configured of current switches, each of which includes resistors R, 2R and P-N-P transistors, is a D/A converter of 4 bits, which supplies a current comparison circuit 11 with 16 values of currents in accordance with the magnitudes of the voltages of the terminals A_1 - A_8 or B_1 - B_8 relative to a power source voltage V_{BB}. That is, letting I_o denote the value of the output current of the single synapse, the following holds:

$$I_0 = \frac{V_{EE}}{R}\left(\frac{A_8^*}{2} + \frac{A_4^*}{2^2} + \frac{A_2^*}{2^3} + \frac{A_1^*}{2^4}\right) \quad (2)$$

In the above formula, A_1^* - A_8^* denote variables which become "1" when the input voltages of the terminals A_1 - A_8 from another neuron are respectively greater than the voltage V_{BB}, and which become "0" when they are respectively smaller.

The current comparison circuit 11 is constructed of a voltage comparator 111 and resistors $\underline{r}$, and it has the nodes of an inverting input (-) and a noninverting input (+). It delivers an output of high voltage ("H") when the current of the noninverting input is more than that of the inverting input, and it delivers an output of low voltage ("L") when the current of the noninverting input is less than that of the inverting input. By the way, the voltage H is set to be sufficiently greater than the power source voltage V_{BB}, while the voltage L is set to be sufficiently smaller than the voltage V_{BB}.

In connecting the other neuron outputs to the synapse, they are connected to the appropriate combination of the input terminals A_1 - A_8 or B_1 - B_8, whereby desired ones of the 16 weights can be selected.

Moreover, since the output of this synaptic circuit is the current, such synaptic circuits may merely be connected in series for an increased number of synapses.

Figs. 6(a) - 6(c) illustrate a model for the synapses and neuron shown in Fig. 5.

Fig. 6(a) is a model diagram showing the synaptic circuit 2 in Fig. 5 in a simplified form. Numerals 8, 4, 2 and 1 denote the input terminals A_8, A_4, A_2 and A_1, respectively, and symbol I_{OUT} denotes the current output of the synapse.

Besides, Fig. 6(b) is a symbolic diagram showing an example of a neural network which adopts the neuron circuit in Fig. 5, and two neurons are used here. Numerical values affixed to the synapses in the figure signify the absolute values of the weights of the corresponding synapses.

The first neuron receives an exitatory input of weight 5 from another neuron (I_{n1}) and one of weight 10 from still another (I_{n2}), and it further receives an inhibitory input of weight -12 from the second neuron. On the other hand, the second neuron receives an excitatory input of weight 9 from another neuron (I_{n3}), and it receives

an inhibitory input of weight -3 from another neuron (I_{n4}) and one of weight -8 from the first neuron. Respective outputs OUT1 and OUT2 from the first and second neurons are sent to other neurons.

Fig. 6(c) is a connection diagram in which the neural network in the symbolic diagram of fig. 6(b) is expressed with the symbol in Fig. 6(a).

First, a common current node to which the first and second synapses are connected in series is coupled to the (+) terminal of the first neuron, and a current node to which the third synapse is connected is coupled to the (-) terminal thereof. The outputs from the other neuron I_{n1} are connected to the terminals A_1 and A_4 of the first synapse, whereby a (+) voltage is input in accordance with a weight of 1 + 4 = 5, and the outputs from the other neuron I_{n2} are connected to the terminals A_2 and A_8, whereby a (+) voltage is input in accordance with a weight of 2 + 8 = 10. Besides, the outputs from the second neuron are connected to the terminals A_4 and A_8 of the third synapse, whereby a (-) voltage is input in accordance with a weight of 4 + 8 = 12.

On the other hand, a common current node to which the first and second synapses are connected in series is coupled to the (-) terminal of the second neuron, and a current node to which the third synapse is connected is coupled to the (+) terminal thereof. The output from the first neuron is connected to the terminal A_8 of the first synapse, whereby a (-) voltage is input in accordance with the weight of 8, and the outputs from the other neuron I_{n4} are connected to the terminals A_1 and A_2 of the second synapse, whereby a (-) voltage is input in accordance with a weight of 1 + 2 = 3. Besides, the outputs from the other neuron I_{n3} are connected to the terminals A_1 and A_8 of the third synapse, whereby a (+) voltage is input in accordance with a weight of 1 + 8 = 9.

By the way, each of the synaptic circuits in Fig. 5 is constructed of the current switch circuit which employs the resistors R, 2R and the P-N-P transistors. Of course, however, any other circuit can be used quite similarly as long as it is the D/A converter of the current output type.

Further, although the number of the input terminals of the synapse is four, that is, the weight is expressed by 4 bits in Fig. 5 and Figs. 6(a) - 6(c), the number of bits can be determined at will.

In this manner, with this embodiment, when a neural network model is to be constructed on a semiconductor integrated circuit, the weights of synapses used in the model can be corrected in a procedure similar to that of a gate array.

As described above, according to the present invention, current values corresponding to synaptic weights can be readily altered by voltages applied externally, and it is therefore permitted to construct a neuron circuit which is easy of altering a learned content and which is suited to a monolithic IC.

Moreover, the summation of the current values corresponding to the synaptic weights is held constant by another regulated current source, and it is therefore permitted to construct a neuron circuit in which the summation of the synaptic weights is held constant without fail.

Claims

1. A circuit for constructing a neural network model, comprising a differential amplifier (11) having an output terminal and two differential input terminals, an excitatory synapse circuit (2-1) connected to the non-inverting input terminal of said differential amplifier (11), and an inhibitory synapse circuit (2-2) connected to the inverting input terminal of said differential amplifier (11),

   characterised in

   that the neural network model constructing circuit is constituted by a semiconductor integral circuit, and

   that each of said excitatory and inhibitory synapse circuits includes a plurality of current switches (Q_{i1}, Q_{i2}), a regulated current source array (3) configured of regulated current source circuits (Q_{sl},r) being equal in number of said current switches (Q_{i1},Q_{i2}) and dètermining values of currents to flow through said current switches, and one load resistor (R) connected to all of said current switches,

   input terminals (P_l) of each said synapse circuit (2) being constructed of terminals which turn "on" and "off" the respective current switches (Q_{i1}, Q_{i2}) and to which external inputs or outputs of another circuit are connected,

   said regulated current source circuits (Q_{sl},r) having current values which can be respectively altered by voltages externally applied independently of one another.

2. The circuit of claim 1, wherein each said regulated current source circuit includes a MOS transistor (Q_{sl}) with a floating gate and a resistor (r), a pulse voltage being impressed on said floating gate of said MOS transistor to control the value of current which said regulated current source circuit causes to flow.

3. The circuit of claim 1 or 2, wherein in said regulated current source array (3), a summation current which all of said regulated current source circuits (Q_{sl}) included therein cause to flow is held constant by a single regulated current source (V_{EE}) which is separately provided.

4. The circuit of any one of Claims 1 to 3, wherein said regulated current source array (3) includes a plurality of transistors (Q_{sl}) whose emitter areas differ in accordance with the values of currents to be respectively caused to flow.

5. The circuit of any one of claims 1 to 4, wherein each said current switch includes one pair of transistors (Q_{l1}, Q_{l2}) and resistors (r_d) which are connected in series with emitters of the respective transistors, and said resistors are constructed of resistors, such as pinch resistors, whose resistances can be altered by an external voltage (V_d) or the like.

6. The circuit of any one of claims 1 to 5, wherein the signal from the output terminal of said differential amplifier (11) is not endowed with a saturation characteristic, whereas the input terminals (P_l) of said synapse circuits (2-1, 2-2) are endowed with saturation characteristics.

Patentansprüche

1. Schaltung zum Aufbau eines neuralen Netzwerksmodells, umfassend einen Differenzverstärker (11) mit einer Ausgangsklemme und zwei Differenz-Eingangsklemmen, einen an die nicht-invertierende Eingangsklemme des Differenzverstärkers (11) angeschlossenen Erregungs-Synapsenschaltkreis (2-1) und einen an die invertierende Eingangsklemme des Differenzverstärkers (11) angeschlossenen Hemmungs-Synapsenschaltkreis (2-2),
   dadurch **gekennzeichnet,**
   daß die Schaltung zum Aufbau eines neuralen Netzwerksmodells von einer integrierten Halbleiterschaltung gebildet ist,
   daß sowohl der Erregungs- als auch der Hemmungs-Synapsenschaltkreis mehrere Stromschalter (Q_{l1},Q_{l2}), eine geregelte Stromquellengruppe (3), die aus geregelten Stromquellen-Schaltkreisen (Q_{sl}, r) konfiguriert ist, deren Anzahl gleich der der Stromschalter (Q_{l1}, Q_{l2}) ist und die Werte von die Stromschalter durchsetzenden Strömen bestimmen, sowie einen mit sämtlichen Stromschaltern verbundenen Lastwiderstand (R) aufweist,
   wobei Anschlüsse (P_l) jedes Synapsenschaltkreises (2) von Anschlüssen gebildet sind, die die betreffenden Stromschalter (Qi_1, Q_{l2}) "ein"- und "aus"-schalten und mit denen externe Eingänge oder Ausgänge einer weiteren Schaltung verbunden sind, und
   wobei die geregelten Stromquellen-Schaltkreise (Q_{sl}, r) Stromwerte haben, die sich jeweils unabhängig voneinander durch extern angelegte Spannungen ändern lassen.

2. Schaltung nach Anspruch 1, wobei der geregelte Stromquellen-Schaltkreis MOS-Transistoren (Q_{sl}) mit einem potentialfreien Gate und einen Widerstand (r) aufweist, und wobei dem potentialfreien Gate des MOS-Transistors eine Impulsspannung zur Steuerung des Stromwertes aufgeprägt ist, den der geregelte Stromquellen-Schaltkreis fließen läßt.

3. Schaltung nach Anspruch 1 oder 2, wobei in der geregelten Stromquellengruppe (3) ein Summenstrom, den sämtliche darin enthaltenen geregelten Stromquellen-Schaltkreise (Q_{sl}) fließen lassen, durch eine einzelne, separat vorgesehene geregelte Stromquelle (V_{ee}) konstant gehalten ist.

4. Schaltung nach einem der Ansprüche 1 bis 3, wobei die geregelte Stromquellengruppe (3) mehrere Transistoren (Q_{sl}) aufweist, deren Emitterbereiche sich entsprechend den Stromwerten unterscheiden, die die jeweiligen Stromquellen fließen lassen.

5. Schaltung nach einem der Ansprüche 1 bis 4, wobei jede Stromquelle ein Paar von Transistoren (Q_{l1}, Q_{l2}) sowie mit den Emittern der jeweiligen Transistoren in Serie geschaltete Widerstände (r_d) aufweisen, und wobei die Widerstände aus solchen Widerständen, etwa Pinch-Widerständen, aufgebaut sind, deren Widerstandswerte sich durch eine externe Spannung (V_d) oder dergleichen ändern lassen.

6. Schaltung nach einem der Ansprüche 1 bis 5, wobei das Signal von der Ausgangsklemme des Differenzverstärkers (11) nicht mit einer Sättigungscharakteristik, die Eingangsklemmen (P_l) der Synapsenschalt-

kreise (2-1, 2-2) dagegen mit Sättigungscharakteristik versehen sind.

Revendications

1. Circuit pour construire un modèle de réseau neuronal, comprenant un amplificateur différentiel (11) possédant une borne de sortie et deux bornes d'entrée différentielles, un circuit de synapse d'excitation (2-1) connecté à la borne d'entrée non inverseuse dudit amplificateur différentiel (11), et un circuit de synapse d'inhibition (2-2) connecté à la borne d'entrée inverseuse dudit amplificateur différentiel (11),

   caractérisé en ce que

   le circuit constituant le modèle de réseau neuronal est constitué par un circuit intégré à semiconducteurs, et

   que chacun desdits circuits de synapse d'excitation et d'inhibition comprend une pluralité d'interrupteurs de courant (Q_{l1}, Q_{l2}), un réseau (3) de sources de courant régulées constituées par des circuits formant sources de courant régulées (Q_{sl},r) qui sont présentes en un nombre égal à celui desdits interrupteurs de courant (Q_{l1},Q_{l2}) et déterminent des valeurs de courant devant traverser lesdits interrupteurs de courant, et une résistance de charge (R) connectée à tous lesdits interrupteurs de courant,

   des bornes d'entrée (P_l) de chacun desdits circuits de synapse (2) étant constituées par des bornes qui placent à l'état "fermé" et à l'état "ouvert" les interrupteurs de courant respectifs (Q_{l1},Q_{l2}) et auxquelles sont connectées des entrées ou des sorties externes d'un autre circuit,

   lesdits circuits formant sources de courant régulées (Q_{sl},r) possédant des valeurs de courant, qui peuvent être respectivement modifiées par des tensions appliquées de l'extérieur, indépendamment les unes des autres.

2. Circuit selon la revendication 1, dans lequel chacun desdits circuits formant sources de courant régulées comprend un transistor MOS (Q_{sl}) possédant une grille flottante et une résistance (r), une tension impulsionnelle étant appliquée à ladite grille flottante dudit transistor MOS pour commander la valeur du courant que fait circuler ledit circuit formant source de courant régulée.

3. Circuit selon la revendication 1 ou 2, dans lequel dans ledit réseau (3) de sources de courant régulées, un courant de sommation, que font circuler tous lesdits circuits formant sources de courant régulées (Q_{sl}) contenus dans le réseau, est maintenu constant par une seule source de courant régulée (V_{EE}), qui est prévue séparément.

4. Circuit selon la revendication 1 à 3, dans lequel ledit réseau (3) formé de sources de courant régulées comprend une pluralité de transistors (Q_{sl}), dont les zones d'émetteur diffèrent en fonction des valeurs de courants devant être respectivement amenés à circuler.

5. Circuit selon l'une quelconque des revendications 1 à 4, dans lequel chacun desdits interrupteurs de courant comprend un couple de transistors (Q_{l1}, Q_{l2}) et des résistances (r_d), qui sont branchées en série avec les émetteurs des transistors respectifs, et lesdites résistances sont constituées de résistances telles que des résistances de pincement, dont les valeurs résistives peuvent être modifiées par une tension extérieure (V_d) ou analogue.

6. Circuit selon l'une quelconque des revendications 1 à 5, dans lequel le signal délivré par la borne de sortie dudit amplificateur différentiel (11) n'est pas doté d'une caractéristique de saturation, tandis que les bornes d'entrée (P_l) desdits circuits de synapse (2-1, 2-2) sont dotées de caractéristiques de saturation.

FIG. 1(a)

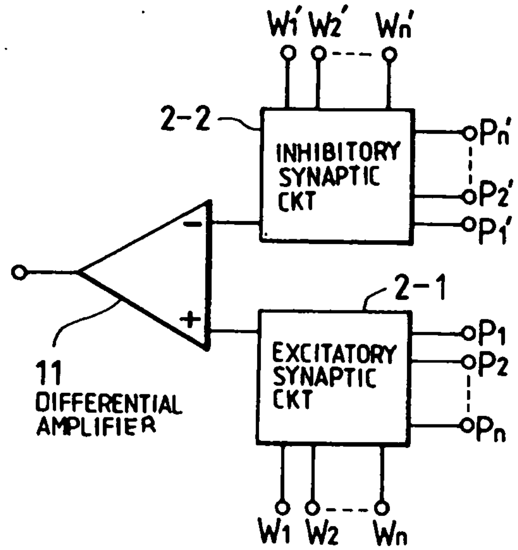

W1' W2' Wn'
2-2
INHIBITORY SYNAPTIC CKT
Pn'
P2'
P1'
2-1
EXCITATORY SYNAPTIC CKT
P1
P2
Pn
11 DIFFERENTIAL AMPLIFIER
W1 W2 Wn

FIG. 1(b)

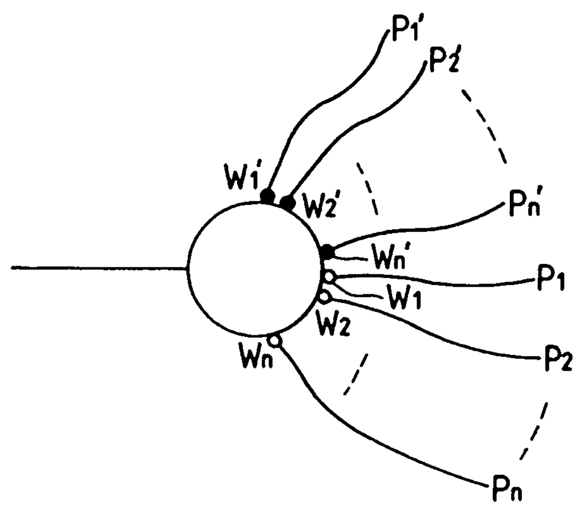

P1'
P2'
W1'
W2'
Pn'
Wn'
P1
W1
W2
P2
Wn
Pn

FIG. 1(c)

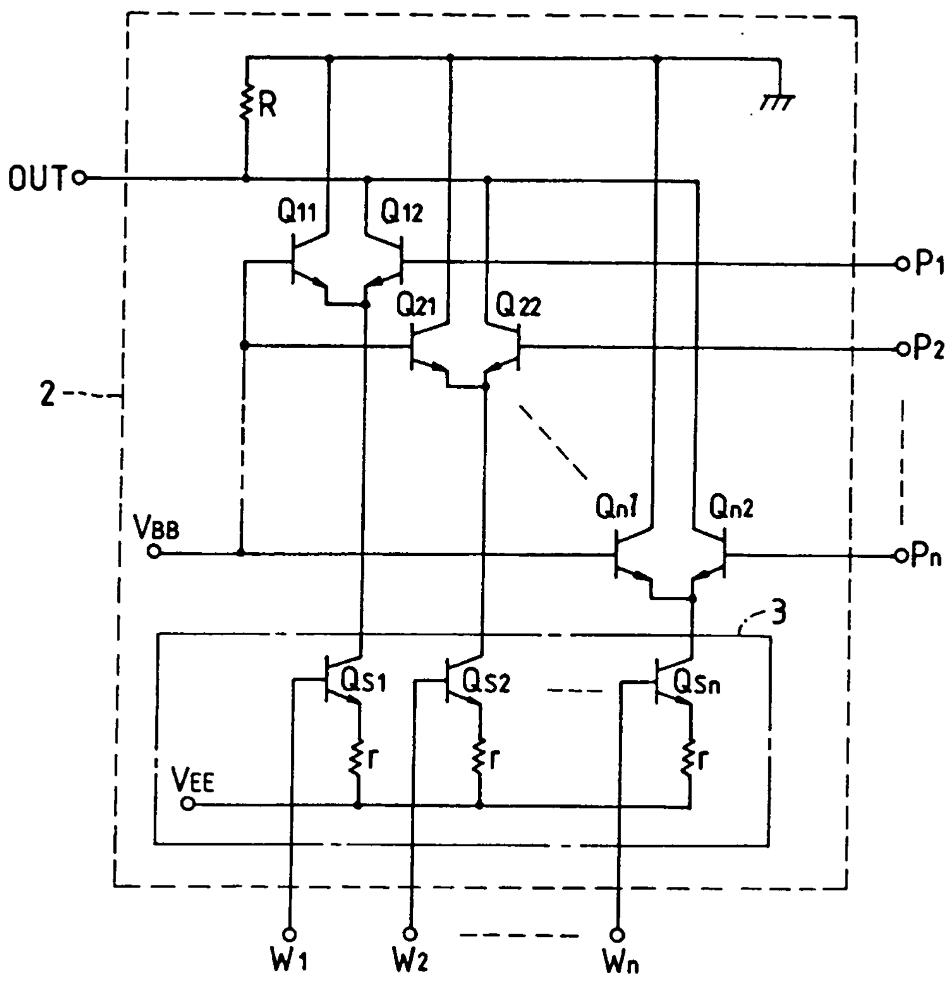

R
OUT
Q11
Q12
P1
Q21
Q22
P2
2
Qn1
Qn2
VBB
Pn
3
Qs1
Qs2
Qsn
r
r
r
VEE
W1
W2
Wn

FIG. 1(d)

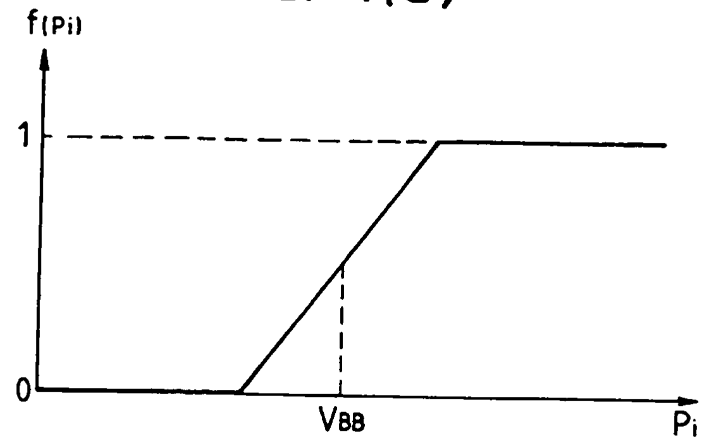


FIG. 1(e)

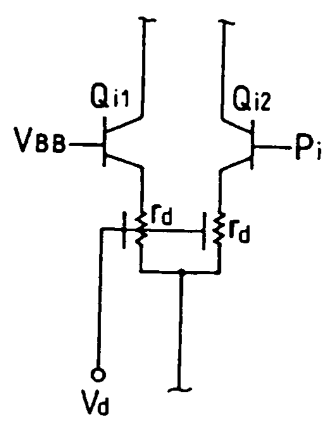


FIG. 2

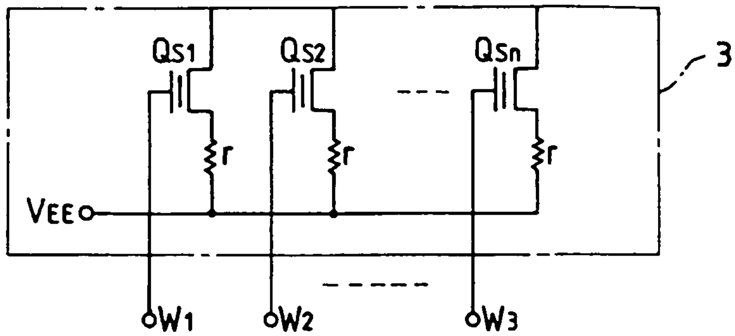

Qs1
Qs2
Qsn
3
r
r
r
VEE
W1
W2
W3

FIG. 3

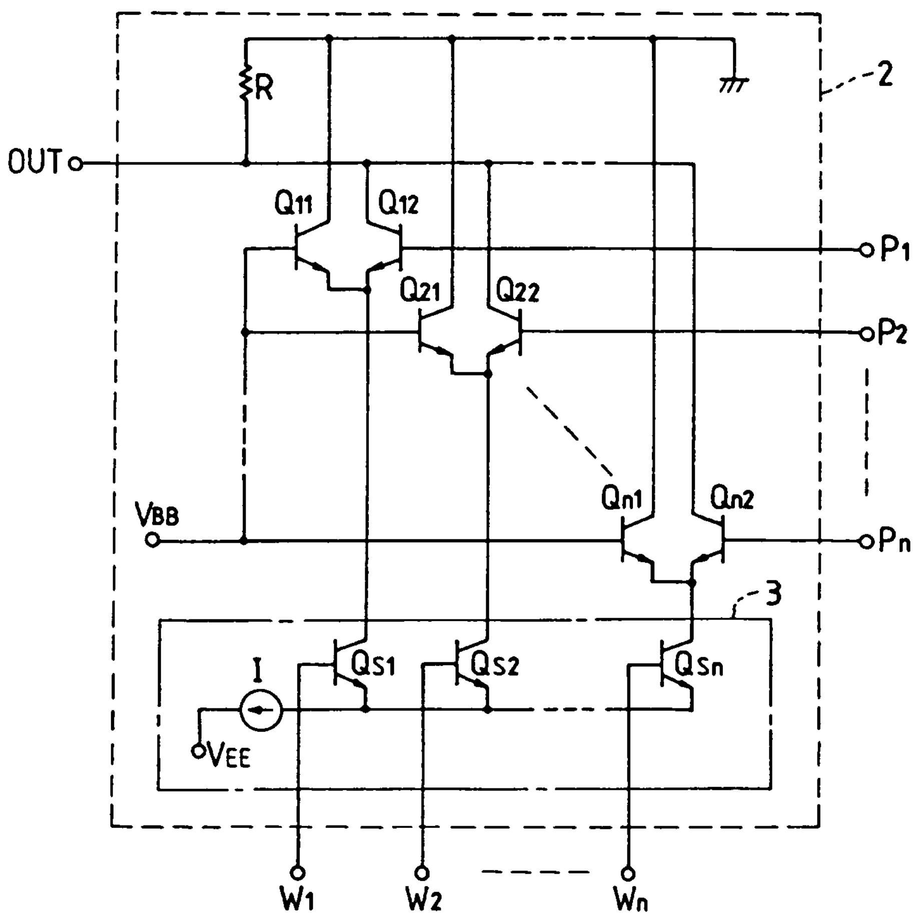
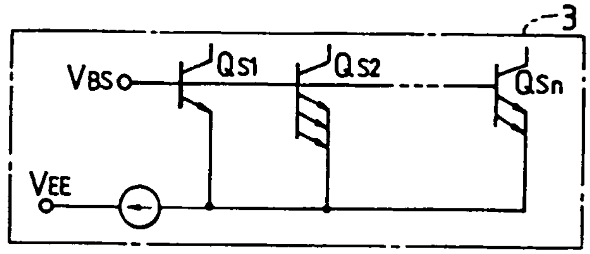

R
2
OUT
Q11
Q12
P1
Q21
Q22
P2
VBB
Qn1
Qn2
Pn
3
I
Qs1
Qs2
Qsn
VEE
W1
W2
Wn

FIG. 4


3
VBS
QS1
QS2
QSn
VEE

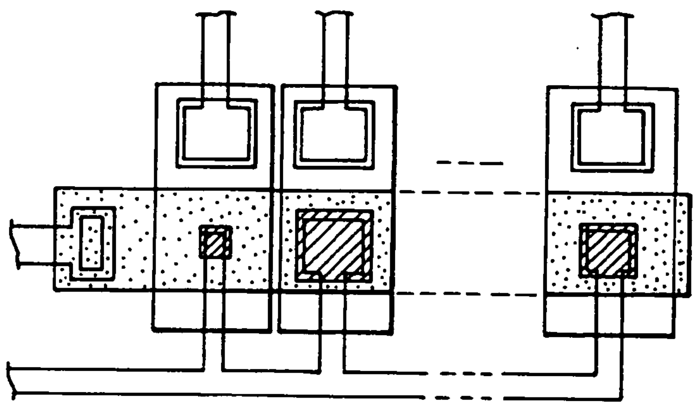


FIG. 8

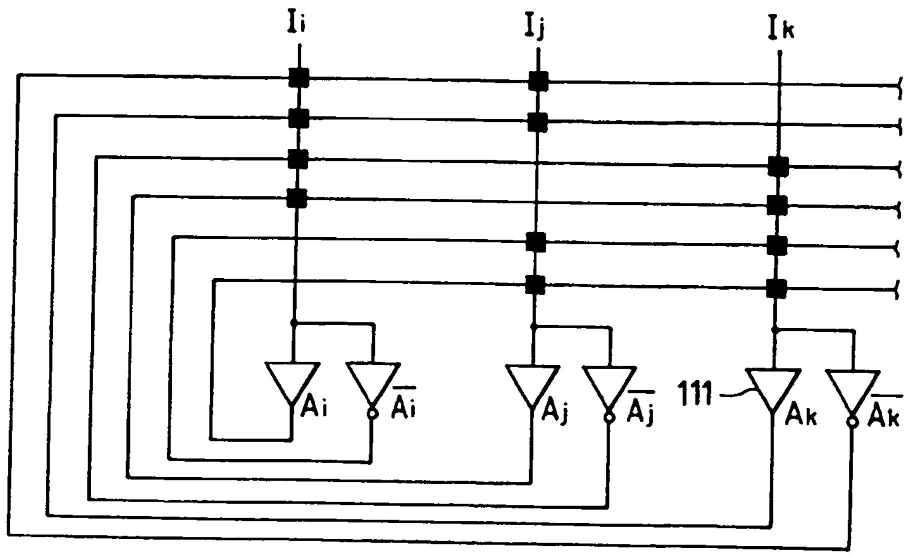

Ii
Ij
Ik
Ai
$\overline{Ai}$
Aj
$\overline{Aj}$
111
Ak
$\overline{Ak}$

FIG. 5

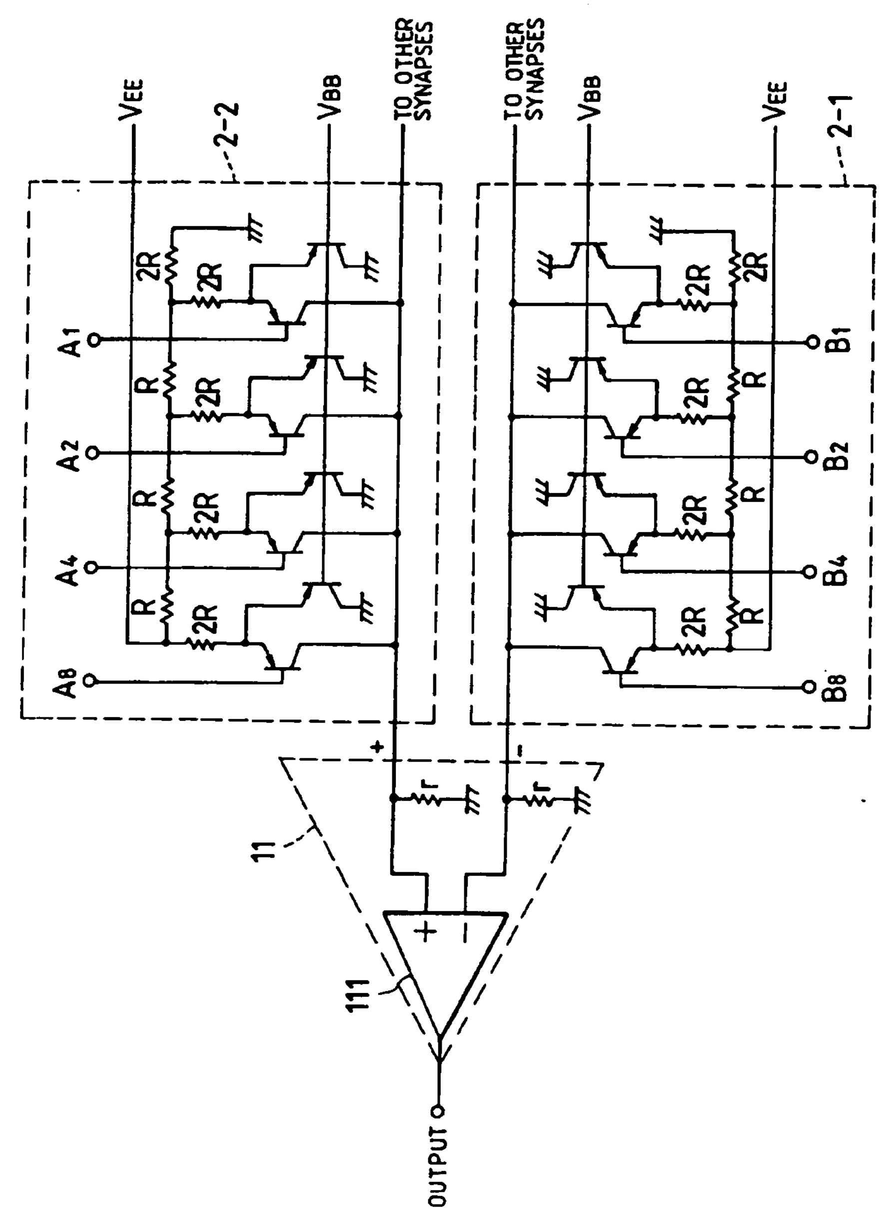

VEE
VBB
TO OTHER SYNAPSES
2-2
2-1
A1
A2
A4
A8
B1
B2
B4
B8
R
2R
r
11
111
OUTPUT

FIG. 6(a)

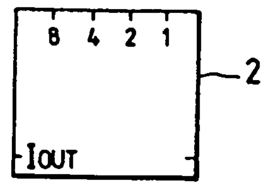


FIG. 6(b)

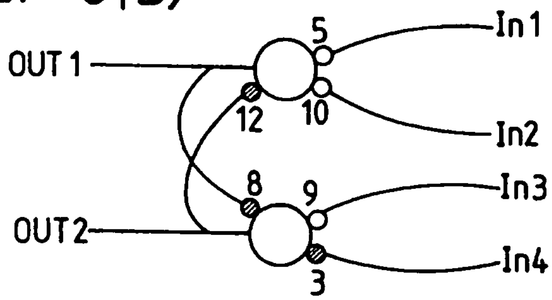


FIG. 6(c)

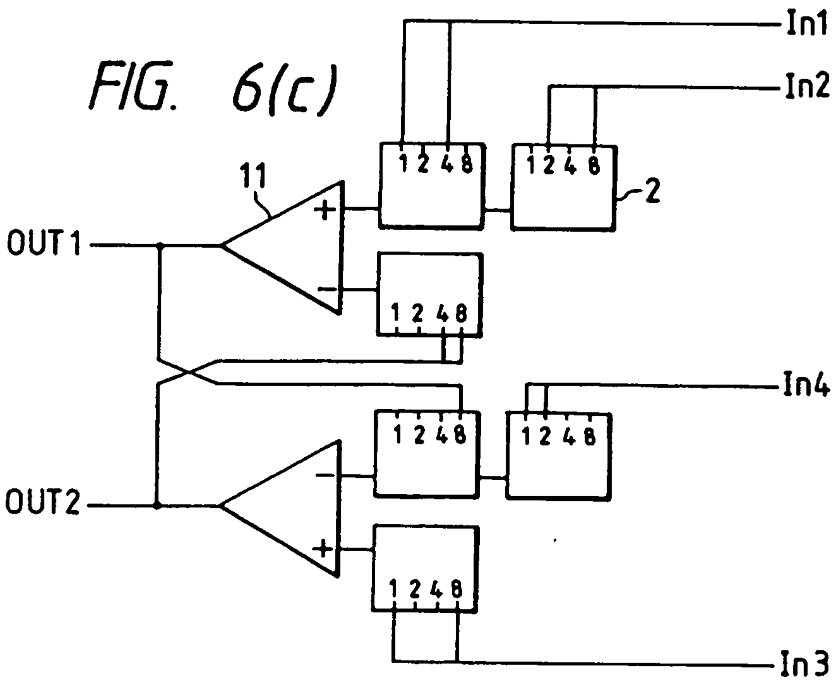


FIG. 7(a)

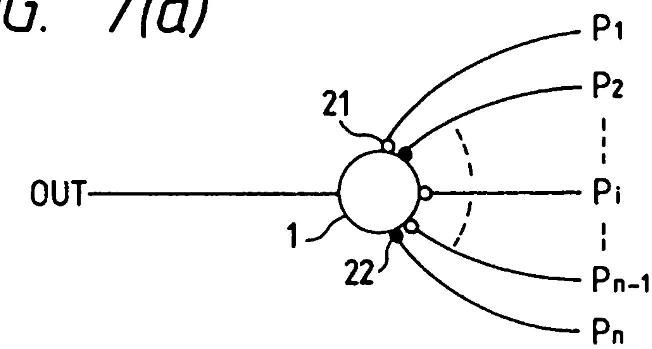
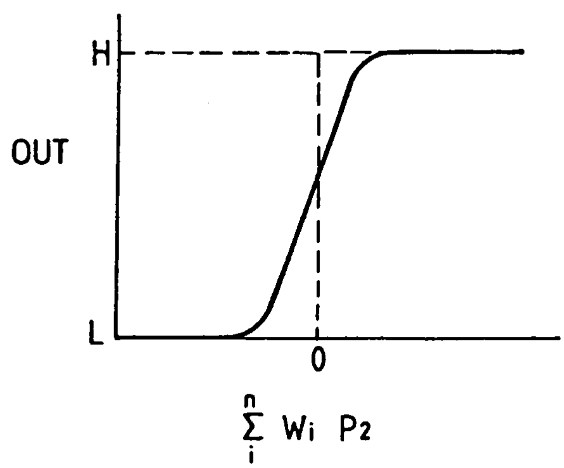


FIG. 7(b)



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